What is claimed is:

1. A method of manufacturing a semiconductor device having a first region, in which a capacitance component is a dominant cause of a RC delay, and a second region, in which a resistance component is a dominant cause of a RC delay, comprising:

performing a first etching process to an insulating layer formed on a semiconductor substrate, so that a first trench having a first thickness and a second trench having the first thickness are formed in the first region and the second region, respectively;

performing a second etching process to the second trench, so that a third trench having a second thickness thicker than the first thickness is formed in the second region;

filling the first trench and the third trench with a metal layer; and

removing portions of the metal layer, so that a first metal interconnection and a second metal interconnection are formed inside of the first trench and the third trench, respectively.

2. The method of claim 1, wherein the metal layer is formed using copper.

3. The method of claim 2, wherein the metal layer of copper is formed using an electroplating method.

4. The method of claim 1, wherein the portions of the metal layer are removed using chemical mechanical polishing (CMP).

5. A method of manufacturing a semiconductor device having a first region, in which a capacitance component is a dominant cause of a RC delay, and a second region, in which a resistance component is a dominant cause of a RC delay, comprising:

forming a mask layer on an insulating layer formed on a semiconductor substrate;

forming a first photoresist layer pattern on the mask layer, so that a portion of the mask layer formed in the first region and a portion of the mask layer formed in the second region are exposed;

performing a first etching process using the first photoresist layer pattern as an etching mask, so that a mask layer pattern, in which the first region and the second region are exposed, is formed, and a first trench having a first thickness and a second trench having the first thickness are formed in the first region and the second region, respectively;

removing the first photoresist layer pattern;

forming a second photoresist layer pattern, with which the first trench of the first region is covered and in which the second trench and portions of the mask layer pattern are exposed;

performing a second etching process using the second photoresist layer pattern and the mask layer pattern as an etching mask, so that a third trench having a second thickness thicker than the first thickness is formed in the second region;

removing the second photoresist layer pattern;

filling the first trench and the third trench with a metal layer; and

removing portions of the metal layer, so that a first metal interconnection and a second metal interconnection are formed inside of the first trench and the third trench, respectively.

6. The method of claim 5, wherein the metal layer is formed using copper.

7. The method of claim 6, wherein the metal layer of copper is formed using an electroplating method.

8. The method of claim 5, wherein the portions of the metal layer are removed using chemical mechanical polishing (CMP).